

Single-Phase 15-Level Switched-Capacitor Boost Multilevel Inverter Topology for Renewable Energy Applications

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Abstract

The integration of multilevel inverter technologies with renewable energy systems has become a focal point for enhancing power quality and conversion efficiency. This paper presents a novel single-phase 15-level switched-capacitor boost multilevel inverter (SC-MLI) topology designed to provide high voltage gain, reduced circuit complexity, and improved harmonic performance. Unlike conventional multilevel inverters, the proposed SC-MLI eliminates the need for an external DC–DC boost converter by incorporating a switched-capacitor mechanism within the inverter stage. The topology generates fifteen discrete voltage levels using a minimal number of switches and capacitors, resulting in a reduced component count and enhanced system efficiency. A notable feature of this design is its inherent self-voltage balancing capability, which maintains capacitor voltage stability without the use of additional sensors or complex control algorithms. MATLAB Simulation confirm that the proposed inverter achieves a high voltage gain and maintains a low total harmonic distortion (THD) below 3.5%, in accordance with IEEE 519 standards. The SC-MLI demonstrates reliable performance under varying load conditions, making it a suitable solution for both grid-connected and standalone renewable energy applications such as photovoltaic (PV) and fuel cell systems. The proposed system is driven with conventional PI and fuzzy controllers. Fuzzy controller shows better results than PI controller in terms of improving power quality and improve power factor to unity.

Keywords: Switched-capacitor inverter, multilevel inverter, voltage boosting, harmonic distortion, renewable energy, PV integration, THD.

I. Introduction

The increasing demand for clean and sustainable energy has accelerated the global transition toward renewable energy sources such as photovoltaic (PV) systems and fuel cells.

These sources, while environmentally friendly, often produce low-voltage and intermittent outputs, necessitating efficient and reliable power conversion systems for grid integration or standalone operation [1]–[3]. Power electronic converters, particularly inverters, play a crucial role in this energy conversion process by transforming DC power from renewable sources into grid-compatible AC voltage [4]. Traditional two-level voltage source inverters (VSIs) are widely used due to their simple structure and ease of implementation. However, they suffer from high switching losses, poor output waveform quality, and elevated total harmonic distortion (THD), which limit their applicability in high-performance systems [5], [6]. To overcome these limitations, multilevel inverter (MLI) topologies have been introduced, offering improved power quality, reduced harmonic content, and lower voltage stress on switching devices [7], [8]. Popular MLI configurations include the diode-clamped multilevel inverter (DCMLI) [9], flying-capacitor multilevel inverter (FCMLI) [10], and cascaded H-bridge multilevel inverter (CHB-MLI) [11]. While these topologies provide excellent waveform shaping capabilities, they often require multiple isolated DC sources, complex modulation schemes, and a large number of components, which increase system cost and complexity [12], [13].

To address these challenges, switched-capacitor multilevel inverter (SC-MLI) topologies have gained significant attention in recent years [14]–[16]. SC-MLIs utilize a combination of capacitors and switches to achieve both voltage boosting and multilevel output generation, eliminating the need for an external DC-DC boost converter [17]. This integration not only simplifies the system architecture but also enhances efficiency and reduces overall component count. Recent developments in SC-MLI designs have focused on improving capacitor voltage balancing, reducing THD, and minimizing switch count without sacrificing output levels [18]–[20]. Some topologies employ resonant charging methods or complex pulse-width modulation (PWM) techniques to achieve voltage regulation, but these approaches increase control complexity [21]–[26].

In this paper, a novel single-phase 15-level SC-MLI topology is proposed, which efficiently integrates switched-capacitor techniques within a multilevel structure. The proposed inverter achieves significant voltage gain without the need for an external boost stage, while ensuring automatic self-voltage balancing of capacitors through its inherent switching logic. The topology requires fewer switches and capacitors compared to existing 15-level inverters, leading to reduced hardware complexity and improved reliability. Comprehensive simulations and experimental validations demonstrate the effectiveness of the proposed topology, achieving low THD (<3.5%), high voltage gain, and robust performance under varying load conditions. These attributes make it highly suitable for renewable energy applications, particularly in PV and fuel cell systems, for both grid-connected and standalone configurations.

II. System Description

The block diagram depicted in shows a reactive power compensation system designed to improve power quality at the point of common coupling where nonlinear load connected to grid.

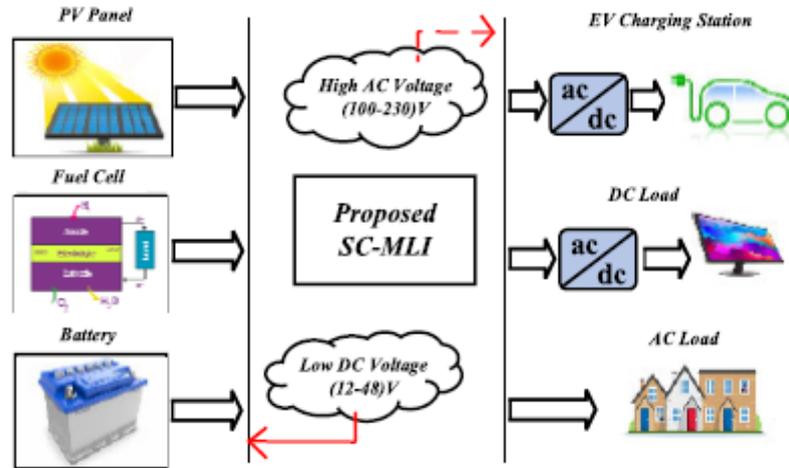


Figure 1:Block diagram of proposed SC-MLI used to interface various sources and loads

A. Proposed Inverter Topology

Multilevel converters are becoming increasingly popular in the industry due to their high-power applications in a variety of systems such as variable speed drives, photovoltaic (PV) grid integration, electric locomotives, power quality improvement devices such as static reactive power compensation, and DVR. In addition to meeting increased power rating and power quality requirements, multilevel inverters also have the ability to eliminate harmonic distortion and the effects of electromagnetic interference. Power sources, and regulating units make up multilevel inverters. Multilevel inverters are frequently utilized these days because of the several benefits they provide, such as lower switching losses, the capacity to operate at high voltages, fewer EMI losses, and improved efficiency .

The primary challenges associated with traditional MLIs are the lack of voltage gain, the requirements for the high number of components to generate higher output voltage, and the number achieved by using a cascaded connection of a single H-bridge. The outcome of the study's effort to reduce the overall element requirement has resulted in many interesting structures, switched capacitor-based multilevel inverter (SC-MLI) is developed to address the issues of classical MLIs by reducing the number of elements with the capability of increasing the output ac voltage.

B. Block Diagram of Switched Capacitor Multi-Level Inverter

A 15-level switched capacitor boost multilevel inverter (SCBMI) is a power conversion topology designed to efficiently convert DC power (from renewable sources like solar panels or wind turbines) into high-quality AC power with multiple voltage levels. This topology integrates switched capacitors to achieve voltage boosting without the need for bulk transformers or additional DC-DC boost converters. Block Diagram Consists of typically, a solar PV array, wind turbine, or battery storage system providing the DC voltage input .

Capacitors are strategically switched to boost the input voltage and stabilize the power. The inverter includes MOSFETs, IGBTs, or other semiconductor devices to control the voltage levels. Controlled by a pulse width modulation (PWM) or multicarrier modulation technique. These capacitor cells are key to voltage boosting. They dynamically charge and discharge to step up the voltage without extra inductors or transformers.

C. Working Principle of 15-Level Inverter:

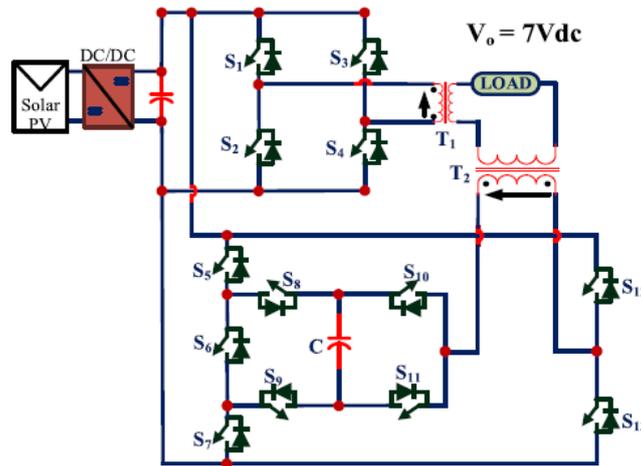


Figure 2: a) Proposed 15-Level SC-MLI fed with solar PV and b) wind energy source.

The Single-Phase 15-Level Switched-Capacitor Boost Multilevel Inverter (SC-MLI) operates on the principle of combining switched-capacitor (SC) techniques with multilevel inverter (MLI) concepts to generate a boosted AC output with multiple voltage levels. The working principle can be explained as follows:

The system typically uses a DC voltage source such as a photovoltaic (PV) array or a battery for renewable energy applications. The switched-capacitor (SC) network is designed to boost the input voltage without the need for an additional step-up transformer or complex DC-DC converter. During specific switching states, capacitors are charged in parallel and discharged in series to achieve voltage boosting.

i) Switching Operation:

The inverter circuit includes multiple semiconductor switches (MOSFETs, IGBTs) that control the charging and discharging cycles of the capacitors. By controlling the switch combinations effectively, the desired voltage levels are generated across the load. The switching sequence is designed to generate output voltages corresponding to different combinations of capacitor voltages and the DC source voltage.

The 15-level output is achieved by combining multiple voltage steps. Each step corresponds to specific capacitor and switch states. For instance, the output voltage steps may

include: $0V$, $\pm V_{dc}/7$, $\pm 2V_{dc}/7$, $\pm 3V_{dc}/7$, ..., $\pm V_{dc}$. The stepped waveform resembles a sinusoidal output with reduced total harmonic distortion (THD).

The switched-capacitor technique enables voltage multiplication by connecting capacitors in series during discharge mode. This results in a boosted voltage greater than the input DC voltage. To achieve a smooth sinusoidal waveform, an LC filter is typically employed at the output stage to reduce high-frequency harmonics and ensure grid or load compatibility.

Figure 2 (b) depicts the proposed inverter configuration used to produce a single AC output voltage, which includes 13 unidirectional switches, one switched capacitor, and two transformers, T1 and T2. The proposed converter produces a 15-level output AC voltage with a voltage gain of 7. The suggested 15-level structure comprises dual voltage boosting components, namely a switching capacitor, C, and a transformer, T1. The switched capacitor, C, is utilized to feed energy to the load symmetrically during the positive and negative cycles, and the voltage across the capacitor remains balanced, demonstrating the proposed MLI's self-balancing capacitor voltage.

ii) Switching States and Operation Modes

The secondary winding of the transformer T1 produces voltage levels of $5V_{dc}$, 0 , $-5V_{dc}$, while the transformer of the second cell T2 generates output voltage with levels of $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$, to produce a peak output voltage of $V_O = 5V_{dc} + 2V_{dc} = 7V_{dc}$. The conduction states for all positive voltage levels of the proposed topology are shown in Fig. 4. and are discussed below:

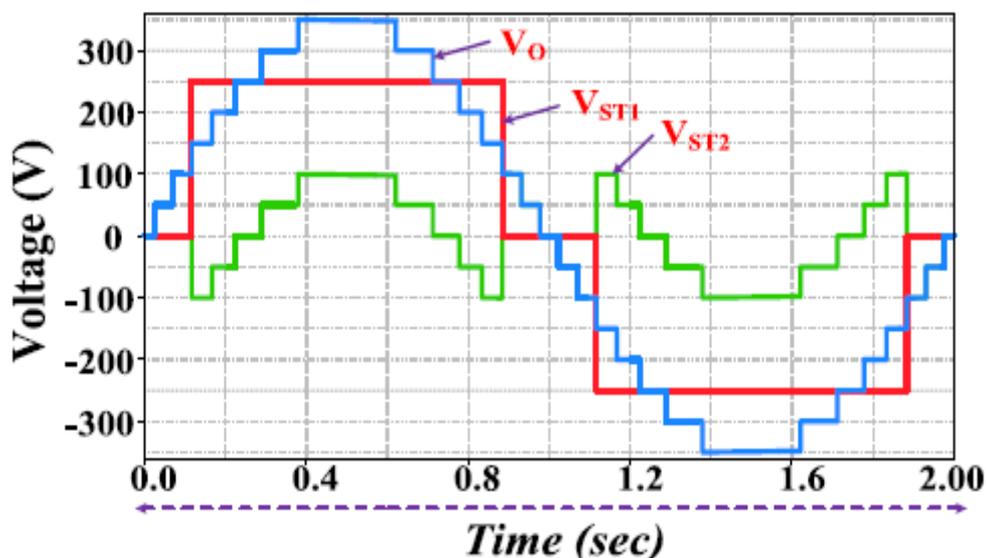
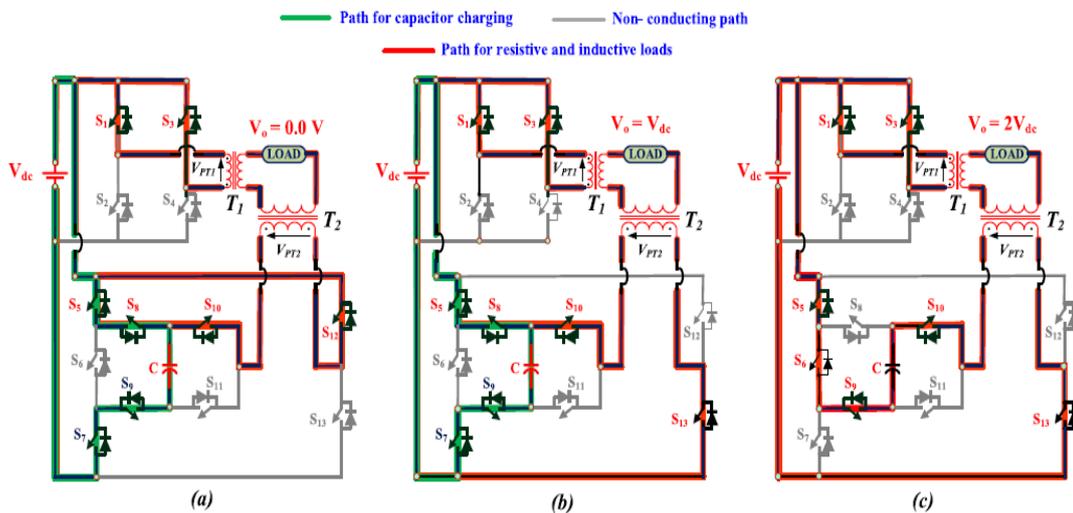


Figure 3: Induced voltage waveforms for VST 1, VST 2 and V_O .

Levels	Switching States	Effect on Capacitor
$+7V_{dc}$	$S_1, S_4, S_5, S_7, S_8, S_{10}, S_{13}$	↓
$+6V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↑
$+5V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{10}, S_{12}$	↑
$+4V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{11}, S_{12}$	↓
$+3V_{dc}$	$S_1, S_4, S_6, S_7, S_9, S_{11}, S_{12}$	↓
$+2V_{dc}$	$S_1, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↓
$+V_{dc}$	$S_1, S_3, S_5, S_8, S_{10}, S_{13}$	↑
0	$S_1, S_3, S_5, S_7, S_8, S_9, S_{10}, S_{12}$	↑
0	$S_1, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{12}$	↑
$-V_{dc}$	$S_1, S_3, S_7, S_9, S_{11}, S_{12}$	↑
$-2V_{dc}$	$S_1, S_3, S_6, S_7, S_8, S_{11}, S_{12}$	↓
$-3V_{dc}$	$S_2, S_3, S_5, S_7, S_8, S_{10}, S_{13}$	↓
$-4V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↓
$-5V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{11}, S_{13}$	↑
$-6V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{11}, S_{12}$	↑
$-7V_{dc}$	$S_2, S_3, S_6, S_7, S_9, S_{11}, S_{12}$	↓

TABLE 1: Switching states of proposed topology



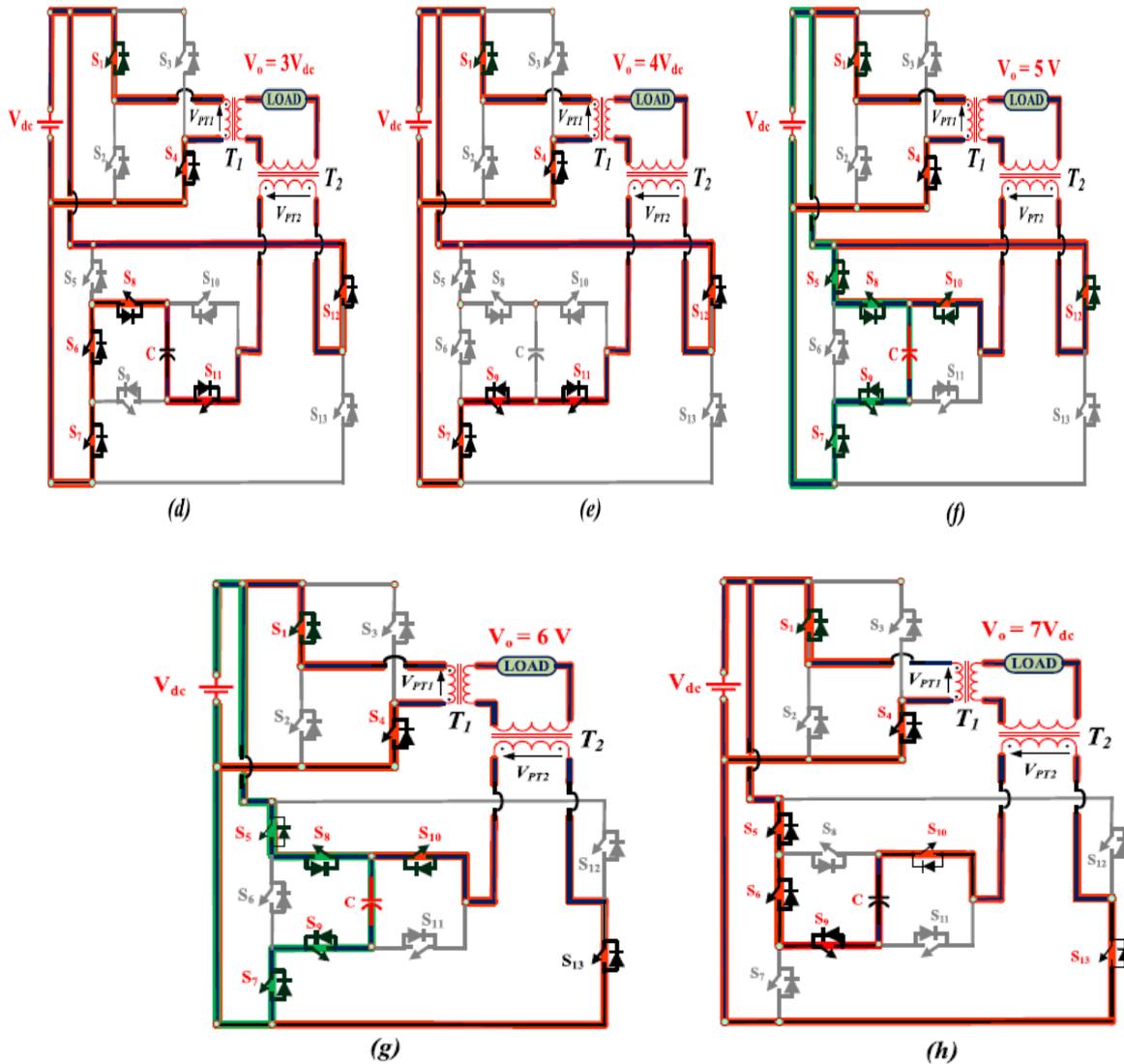


Figure 4: Different stages of the proposed single-stage SC-MLI topology, which produces 15-level ac output voltage.

- State A ($V_{ST1} = 0, V_{ST2} = V_{dc}, V_o = V_{dc}$): In this state, the capacitor, C starts charging, the H-bridge at this stage produces zero power and the output voltage level is produced by the second cell as in Fig. 4(b).
- State B ($V_{ST1} = 0, V_{ST2} = 2V_{dc}, V_o = 2V_{dc}$): During this voltage state, the capacitor, C still discharging, and the output voltage obtained is $2V_{dc}$. The corresponding circuit diagram is shown in Fig. 4(c).
- State C ($V_{ST1} = 5V_{dc}, V_{ST2} = -2V_{dc}, V_o = 3V_{dc}$): The switching diagram for this stage is shown in Fig. 4(d). In this stage, the capacitor, C continues to discharge through the load, and the load voltage level is equal to $3V_{dc}$.
- State D ($V_{ST1} = 5V_{dc}, V_{ST2} = -V_{dc}, V_o = 4V_{dc}$): In this voltage state as shown in Fig.4(e), the capacitor starts discharging and the output voltage level having its peak value equal to $4V_{dc}$ is achieved.

- State E ($V_{ST1} = 5V_{dc}$, $V_{ST2} = 0$, $V_o = 5V_{dc}$): In this operating mode, the capacitor, C still charging through the load, and the output voltage level is generated by the upper H-bridge cell while the lower cell produces zero power as shown in Fig. 4 (f).
- State F ($V_{ST1} = 5V_{dc}$, $V_{ST2} = V_{dc}$, $V_o = 6V_{dc}$): During his operating mode, the capacitor, C starts charging and the series connection of secondaries of T1 and T2 produces a level with a voltage magnitude of $6V_{dc}$ which is shown in Fig.4 (g).
- State G ($V_{ST1} = 5V_{dc}$, $V_{ST2} = 2V_{dc}$, $V_o = 7V_{dc}$): In this operational mode, the proposed topology generates zero voltage across the load as shown in Fig.4 (h). For this state, the capacitor C discharging.
- State O ($V_{ST1} = V_{ST2} = V_o = 0$): As shown in Fig. 4 (a), zero voltage appears across the load, and the capacitor is connected to the DC voltage source and gets charged to V_{dc} . A similar analysis can be applied over the negative half cycle of the output voltage. The switching pattern used to generate a 15-level Output voltage, V_o is presented in Table 1.

iii) **Control Algorithm for Capacitor Balancing:**

Capacitor balancing refers to the process of ensuring that the voltage across each capacitor in a system (particularly in multi-level inverters or energy storage systems) is equal or within a safe margin. If capacitors in parallel or in a series arrangement are not balanced, it can lead to issues such as over-voltage, under-voltage, overheating, or reduced system performance. Therefore, implementing an effective control algorithm for capacitor balancing is crucial for ensuring safe and efficient operation in power electronic systems like multi-level inverters, DC-DC converters, or energy storage systems. Prevent Over-voltage and Under-voltage: Ensure that the voltages across capacitors do not exceed their rated voltage limits or fall too low, which could damage the capacitors or the overall system. Improve Efficiency: By maintaining balanced voltage levels, the system operates more efficiently, preventing excessive power losses and improving the reliability of the power conversion process.

III. Results & Discussion

Simulation Model of Cascaded 15-Level Inverter Based on The Proposed Basic unit. The Simulink diagram you provided appears to be a model of a Multilevel Inverter (MLI), likely related to your project on the 15-level asymmetric multilevel inverter with reduced switch count using different PWM techniques.

The presence of multiple DC sources suggests an asymmetric configuration, where different voltage levels are used to generate the multilevel output. Multiple

IGBTs or MOSFETs are used, arranged in a way that supports reduced switch count topology. Each switch is likely controlled using a PWM technique, such as SPWM, SHEPWM, or PODPWM, to generate the required output waveform. Some sections seem to have capacitors, which might be used for voltage balancing. Clamping diodes could be present if it's a diode-clamped inverter topology. There are logic control blocks in the diagram, which are likely used for PWM signal generation. These signals determine the gate pulses for the semiconductor switches. The output section shows a load, which could be a resistive (R), inductive (RL), or motor load where the multilevel waveform is applied. A 15-level stepped AC waveform, reducing Total Harmonic Distortion (THD) compared to a conventional inverter. Improved power quality due to the asymmetric voltage sources and optimized switching pattern.

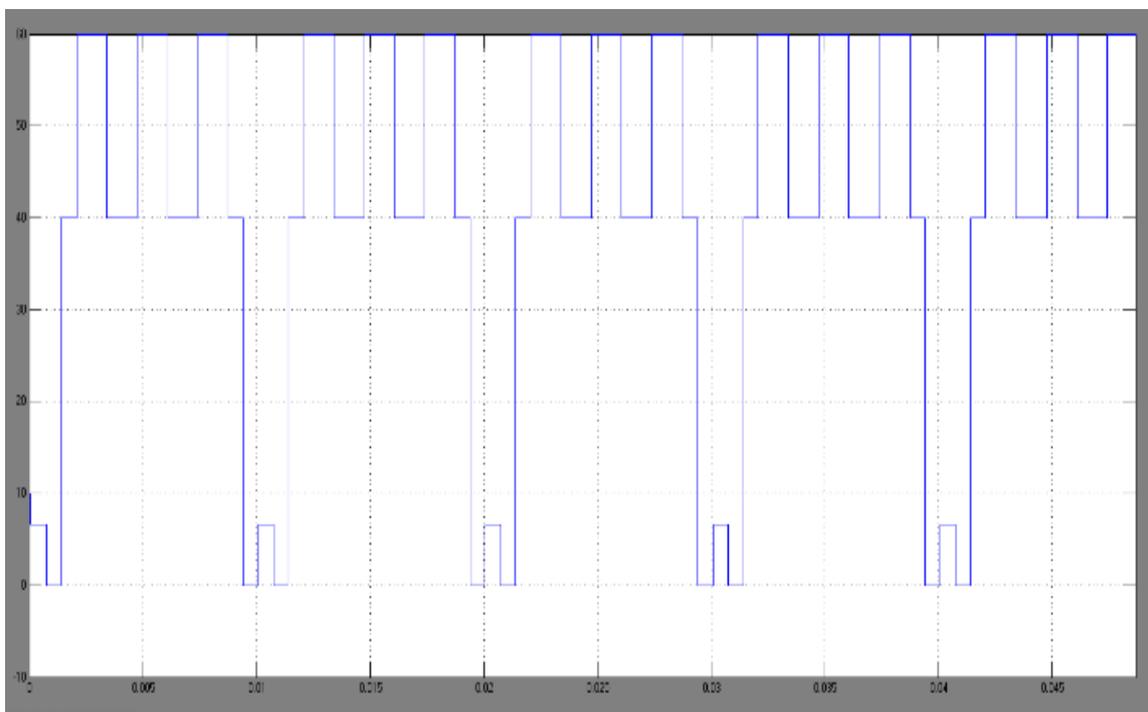


Figure 5: Basic Unit 1 of Voltage (VT1).

Figure 5 represents the waveform of output current or possibly a gate pulse signal of the switches in a single-phase 15-level switched capacitor boost multilevel inverter. The waveform shows periodic switching between two or more discrete levels. This indicates controlled switching of semiconductor devices within the inverter topology. The periodic nature confirms that this is likely associated with the control signals or current response to the stepped voltage output shown in the previous figure. The narrow and wide pulses seen in the waveform might be corresponding to on/off states of switches or to current conduction periods of certain components like capacitors or power devices. The pattern confirms a multi-level stepped strategy rather than a simple two-level inverter, improving harmonic performance.

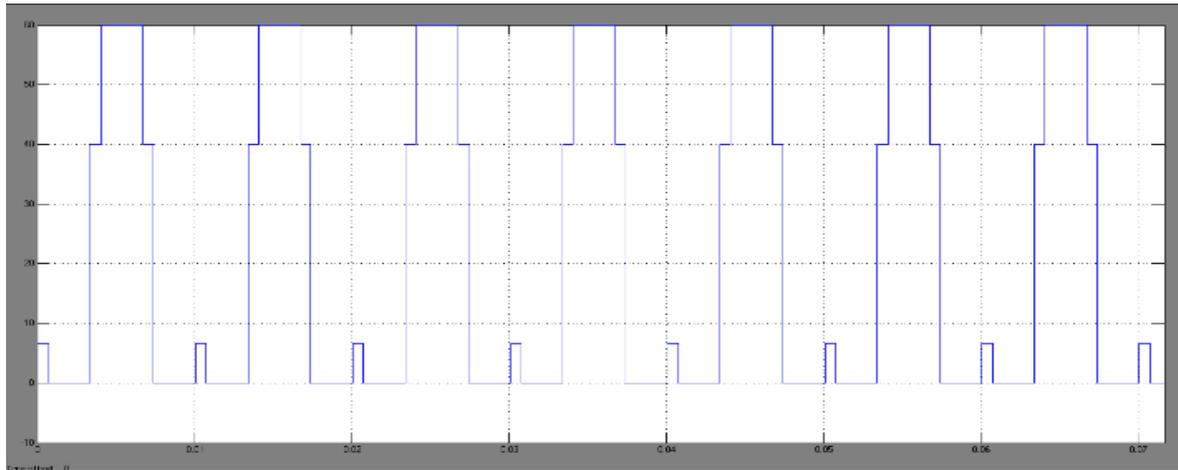


Figure 6: Basic Unit 2 of Voltage (VT2).

The waveform shown in the Figure 6 used to represent the output voltage of the proposed basic unit 2 in your 15-level asymmetric multilevel inverter. The waveform consists of multiple voltage levels, which indicates a multilevel inverter output rather than a simple square wave. The presence of smaller pulses within the main waveform suggests the use of PWM techniques for harmonic reduction.

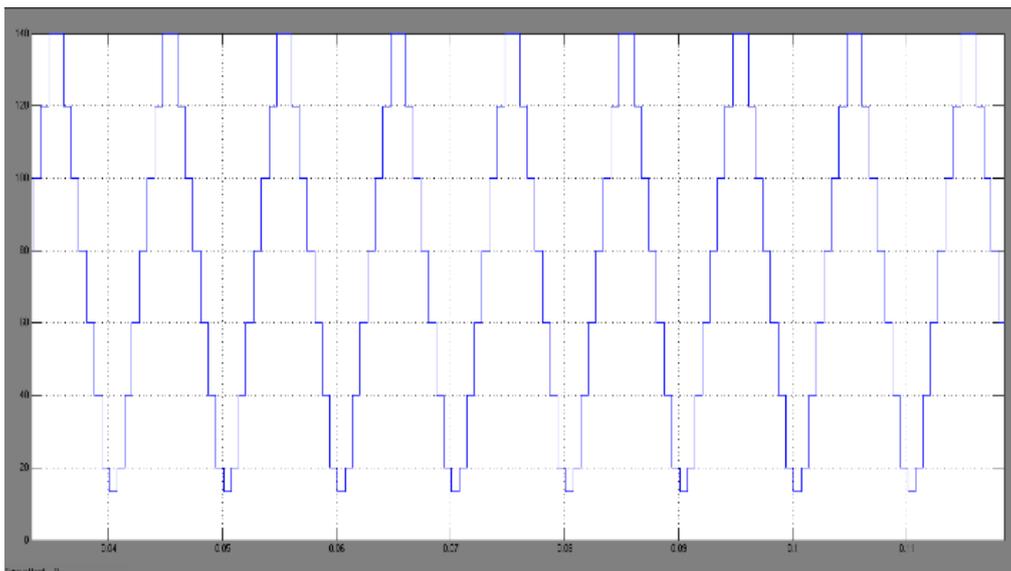


Figure 7: Voltage of V_o which is obtained from VT1 and VT2.

The voltage transitions show multiple steps, which confirms that this is part of an asymmetric inverter topology. The levels might be derived from different DC voltage sources in the circuit. The high-frequency pulses in the waveform indicate modulation using PWM. The waveform's shape suggests that it is a sub-unit contributing to the final 15-level output. This unit likely works in combination with other units to generate the full stepped waveform. The voltage contribution from this unit is crucial in forming the desired multilevel output.

Reduced Total Harmonic Distortion (THD) due to multiple levels. Improved output waveform quality compared to a conventional two-level inverter. More efficient power conversion for applications such as motor drives and renewable energy systems. Figure 7 shows the waveform of Output Voltage and Current of Fifteen Level Inverter Waveform of Single-Phase 15-Level Switched Capacitor Boost Multilevel Inverter Topology for Renewable Energy Applications

IV. Conclusion

The model is designed and analysed its performance on the basis of reactive power compensation and power quality improvement. In this model, PI controller is used. The proposed concept is simulated using MATLAB/Simulink and performance is observed doing THD analysis. From the above results, it is evident that the proposed control strategy for reactive power compensation in improving the power quality, maintaining unity power factor and improved system voltage THD and current THDs compared with the conventional PI controller based control strategy.

References

- [1]. H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*, Wiley, 2014.
- [2]. J. M. Guerrero et al., "Microgrids: An overview of control strategies and decentralized control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 562–575, 2013.
- [3]. B. Wu et al., *Power Conversion and Control of Wind Energy Systems*, Wiley-IEEE Press, 2011.
- [4]. S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [5]. M. Malinowski et al., "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [6]. J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [7]. P. Lezana et al., "Survey of multilevel converter topologies to integrate renewable energy sources into the distribution grid," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1080–1089, Apr. 2011.
- [8]. E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.
- [9]. A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
- [10]. M. F. Escalante, J. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 809–815, Aug. 2002.
- [11]. F. Z. Peng, "A generalized multilevel inverter topology with self-voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, Mar./Apr. 2001.
- [12]. E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.

- [13]. M. Khazraei, H. Sepahvand, and K. Corzine, "H-bridge cascaded multilevel inverter: Analytical approaches to harmonic reduction and voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2564–2574, Jul. 2013.
- [14]. A. R. Reisi et al., "Review of photovoltaic inverter topologies," *Renewable and Sustainable Energy Reviews*, vol. 15, no. 5, pp. 2712–2723, Jun. 2011.
- [15]. S. Rahmani, K. Al-Haddad, and M. Kazerani, "A new single-phase multilevel inverter with reduced number of switches and DC voltage sources," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, Feb. 2012.
- [16]. S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.
- [17]. S. Mekhilef and M. N. A. Kadir, "Voltage control of three-stage hybrid multilevel inverter using vector transformation," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2599–2606, Oct. 2010.
- [18]. R. Stala, "A natural DC-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008–5018, Nov. 2013.
- [19]. P. Alaeinovin and A. Mokhberdorran, "A novel switched capacitor multilevel inverter with reduced components and self-voltage balancing," *IET Power Electron.*, vol. 13, no. 3, pp. 509–519, Mar. 2020.
- [20]. R. Seyezhai and B. L. Mathur, "Harmonic analysis of multicarrier PWM techniques for hybrid multilevel inverter," *Journal of Electrical Engineering*, vol. 60, no. 3, pp. 117–124, 2009.
- [21]. D. Jovcic and K. Ahmed, "High power AC-DC-AC converters with reduced switch count," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2551–2559, Oct. 2010.
- [22]. S. N. Manoharan and S. Radha, "Analysis and implementation of a reduced switch multilevel inverter for photovoltaic applications," *Solar Energy*, vol. 181, pp. 83–92, Mar. 2019.
- [23]. Paramasivan, M., Prasad, T.N. & Vanchinathan, K. Experimental and numerical investigations on amalgamation of mixed frequency carrier based asymmetrical 15 level multilevel inverter. *Electr Eng* **107**, 5861–5875 (2025). <https://doi.org/10.1007/s00202-024-02854-2>.
- [24]. M. Paramasivan *et al.*, "An Alternative Level Enhanced Switching Angle Modulation Schemes for Cascaded H Bridge Multilevel Inverters," in *IEEE Access*, vol. 11, pp. 57365-57382, 2023, doi: 10.1109/ACCESS.2023.3283253.
- [25]. Chinnaraj, G., Kumarasamy, V., Paramasivan, M. *et al.* Mathematical formulation of multicarrier PWM techniques and design an eleven-level modular multilevel inverter to improve power quality. *Int J Syst Assur Eng Manag* **14**, 1218–1227 (2023). <https://doi.org/10.1007/s13198-023-01926-z>
- [26]. B. Kadiyala, P. Muthukumar and R. Bensraj, "Performance Analysis of Fixed and Variable Frequency Multi Shape Carrier-Seven Level Multilevel Inverter," *2021 Innovations in Power and Advanced Computing Technologies (i-PACT)*, Kuala Lumpur, Malaysia, 2021, pp. 1-8, doi: 10.1109/i-PACT52855.2021.9696891.